Method and arrangement for instruction word generation in the driving of functional units in a processor

Abstract

The invention relates to a method and an arrangement for instruction word generation in the driving of functional units in a processor, the instruction words comprising a plurality of instruction word parts. In this case, in a program sequence, under the control of a program word, an instruction word is taken from a row - determined by a reading row number - of an instruction word memory that can be written to row by row, the said instruction word is altered by means of substitution of an instruction word part by the information part of the respective program word and is written back to a row of the instruction word memory, the said row being determined by a writing row number. Afterwards, an instruction word - which is generated in this way and is to be executed in accordance with the program - for driving the functional units is output to the processor.

According to the invention, a reduction in the processing width and an increase in the operating speed is achieved by the writing and reading row numbers being generated by corresponding registers and/or the largest possible number of instruction words that are to be executed being successively compiled in the instruction word memory and processed, so that they are combined in blocks. This makes it possible to reduce the processing width during the program word processing in the part which carries control information.
(Figure 1)